UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,618	10/22/2001	Cynthia M. Merkin	DC-03124	2972

33438 7590 12/12/2008

HAMILTON & TERRILE, LLP
P.O. BOX 203518
AUSTIN, TX 78720

EXAMINER	
DALENCOURT, YVES	
ART UNIT	**PAPER NUMBER**
2457	

NOTIFICATION DATE	DELIVERY MODE
12/12/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tmunoz@hamiltonterrile.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/027,618
Filing Date: October 22, 2001
Appellant(s): MERKIN, CYNTHIA M.

Cynthia M. Merkin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/06/2008 appealing from the Office action mailed 05/19/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

20010044841	Kosugi	11-2001
6,205,547	Davis	3-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the appellant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the appellant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-17, 20, and 22-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Kosugi et al. (US 2001/0044841; Kosugi hereinafter).

With regard to claim 1, Kosugi shows the method comprising: providing a computer system with a system management controller coupled between a processor bus and a local bus [See Fig. 2A, in which the line that represents the bus from the local CPU connects to the item 88 and another local bus]; configuring the system management controller to monitor a task of writing data to an event log, the task being executed by a Basic Input Output System (BIOS) program in response to the failure [See item 88, Fig. 2 for the system management controller. BIOS program is not explicitly spelled out. However, its existence within Kosugi can be inferred from the mention of BIOS log (see paragraph 0029), POST (see paragraph 0029), and the fact that CPU's are Intel Architecture (paragraph 0029) which use BIOS. The task of writing

the log is performed by BIOS program ("BIOS log")]; monitoring the task for completion [See paragraph 0030, which indicates that the system controller is notified of errors in BOOT processing. In other words, it is monitoring BIOS sequence, which includes BIOS logging]; accessing the event data if the task fails to complete [See paragraph 0030. It describes system controller 88 accessing the BIOS log in non-volatile storage in the case of failure]; and writing the event log via the system management controller in response to accessing the event data. The BIOS log in nonvolatile memory 78 is transferred and written to nonvolatile memory 140 of the Server Management Support Board 36. See the end of paragraph 0034.

With regard to claim 3, Kogusi shows that monitoring the task comprises: setting a configurable time of a watchdog timer, the task being configured to access the event data, and write the data to the event log in response to the event data, the task being completed within the configurable time set in the watchdog timer [See Figs. 7A and 7B and paragraph 0035 for the description of IMP board, which acts on behalf of the controller 88. The paragraphs 0035 and 0038 describe "configuring" (or setting) of the timers. The task of writing the event log has been discussed with respect to claim 1. Note that what is being written has to be "event data."]; receiving an indication from the BIOS program on completion of the task [See POST diagnosis UNIT in item 100 ("BIOS") in Fig. 3A. See Fig. 7A for problem notification process. Starting of BOOT (which is started by the BIOS) is used as notification that POST (which includes logging) has terminated].

With regard to claim 4, Kosugi shows that the task fails to complete when the task fails to receive the indication from the BIOS program. See step s4 in Fig. 7A, for when the timer expires before BOOT. See paragraph 0035 for various timer expirations descriptions.

With regard to claim 6, Kosugi shows that the event data is stored in a memory of the computer system by a controller device included in the computer system. See Fig. 2A, which shows the nonvolatile memory 78, which is on the computer system. Paragraph 0034 indicates that the event log is stored in nonvolatile memory 78. Note that CPU, items 64-1, ("controller device") executes BIOS (and thus BIOS logging)].

Claims 7 and 8 refer to two controllers: memory controller and I/0 controller. Kosugi meets the limitations in two ways. First, note that CPU's generally control memory and I/O. Therefore, Kosugi's CPU can be viewed as both memory controller and I/O controller. Second, hardware specific memory controllers and I/O controllers are generally inherent in most motherboards (For example, see descriptions of Intel 865D, which are involved in writing of data to memory. Baseboard in Kosugi corresponds to motherboard].

With regard to claim 9, Kosugi shows that the system management controller accesses the event data over a system bus of the computer system. See Fig. 2A and PCI bus 66 as well as well I2C bus 84-1 and 84-2.

With regard to claim 10, Kosugi shows a SMbus. I2C Bus 84-1 is the SMbus.

With regard to claim 11, Kosugi shows the system management controller writing the event log in response to accessing the event data. The BIOS log in nonvolatile

memory 78 is transferred and written to nonvolatile memory 140 of the Server Management Support Board 36. See the end of paragraph 0034.

With regard to claim 12, Kosugi shows that writing the event log occurs over a system bus of the computer system. See PCI bus 66 in Fig. 6A. Server Management Board 36 is implemented as a PCI board, and therefore it uses PCI bus.

With regard to claim 13, its limitation has been discussed with respect to claim 10.

With regard to claim 14, two of its limitations have not been discussed. They are: configuring the watchdog timer to allow the BIOS program to complete in absence of a second failure. Kosugi shows this limitation in Fig. 7A. The flow chart shows that when a particular failure occurs twice, the steps in Fig. 7A are re-traversed. Specifically, note the path through S1, S2, S3, S5, S8 and S10, and then returning to S1. On the second traversal, the timer will be restarted again at S5; determining whether the execution of the BIOS program caused the second failure, the second failure forcing the watchdog timer to expire. The expiration in S8, Fig. 7A indicates the trouble with booting and BIOS and thus the second failure.

With regard to claim 15, Kosugi shows that the second failure is substantially similar to the first failure. In traversing Fig. 7A diagram, the second failure (which is the same as the first one) will occur again and cause the reboot.

With regard to claim 16, Kosugi shows that the second failure occurs while a processor included in the computer system operates in a SMM mode. System

Management Mode occurs during pre-boot. Fig. 7A shows that the second failure, at the second traversal of the steps in Fig. 7A, occurs prior to the start of the BOOT.

With respect to claim 17, except for amended portions, its limitations substantively restate the limitations of claims 1 and 3-16, but in apparatus form rather than in method form. The reasons for the rejections of claims 1 and 3-16 apply to the unamended portions of the limitations of claim 17.

With respect to claims 17's new limitation, write the data to the event log if the BIOS program has not written the data to the event log, Kosugi meets the limitation, because its data is written to the log whether or not BIOS program has not written data to the event log. In other words, data is still written to the log if BIOS program has not written to the event log.

With respect to claim 20, Kosugi shows the method comprising: monitor a task of writing data to an event log via the system management controller [], the task being executed by a Basic Input Output System (BIOS) program in response to the failure [See item 88, Fig. 2 for the system management controller. BIOS program is not explicitly spelled out. However, its existence within Kosugi can be inferred from the mention of BIOS log (see paragraph 0029), POST (see paragraph 0029), and the fact that CPU's are Intel Architecture (paragraph 0029) which uses BIOS. The task of writing the log is performed by BIOS program ("BIOS log"). "Monitoring" is a generic function that is involved in any program]; monitoring the task for completion to determine whether the BIOS program was able to complete writing the data to the event log [[See paragraph 0030, which indicates that the system controller is notified of errors

in BOOT processing. In other words, it is monitoring BIOS sequence, which includes BIOS logging]; accessing the event data if the task failed to complete [See paragraph 0030. It describes system controller 88 accessing the BIOS log in non-volatile storage in the case of failure]; and writing the event log via the system management controller if the task failed complete [The BIOS log in nonvolatile memory 78 is transferred and written to nonvolatile memory 140 of the Server Management Support Board 36. See the end of paragraph 0034.].

In claim 20, the limitation referring to the system management controller has been discussed with respect to claim 1.

Claims 22-32 incorporate the limitations of corresponding claims 3-13, but in method form, rather than in apparatus form. The reasons for the rejection of claims 3-13 apply to claims 22-32.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 18, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosugi in view of Edward L. Davis (US 6,205,547; hereinafter Davis).

With respect to claim 2, Kosugi does not show that the failure generates a system management interrupt and the BIOS program is triggered in response to the system management interrupt. However, Davis shows the generation of both system interrupt and triggering of the timer interrupt in lines 12-37, column 4. Note that Kosugi shows the failure is written in BIOS log. It would have been one of ordinary skill in the art at the time of the invention to use interrupts to signal failure in Kosugi is that Davis suggests the use of interrupts for error detection in pre-boot operations. See lines 12-37, column 4.

Claims 18 and 19 substantively restate the limitations of claims 1-17, but in apparatus form rather than in method form. The reasons for the rejections of claims 1-17 apply to claims 18 and 19 with respect to its constituent limitations. Note that Davis illustrates timer interrupt being set upon the first failure. The rationale for the obviousness rejection of claim 2 holds for claims 18 and 19.

Claim 21 substantively incorporates the limitations of claim 2, but in different words. The reasons for the rejection of claim 2 apply to claim 21.

(10) Response to Argument

In response to Appellant's argument (page 5) that Kosugi does not disclose monitoring for the failure of a task to complete where the monitoring is via a system management controller that is included within the computer system in which the failure occurs. The Examiner respectfully disagrees with Appellant's assertion because Kosugi discloses the controller 88 in fig. 2, which is local to the system and performs the logging, as is the system controller in claim 1 (see paragraph [0030].

Appellant's argued that Kosugi fails to disclose or suggest that the system management controller is within the system for which the event data is being generated. The Examiner respectfully disagrees with Appellant's remark because the event log recites in the claims corresponds to Kosugi's system log. In Kosugi's system, when the "event log" is written by the "controller", the event log is written to the system log (i.e., BIOS log). In fact, "writing the event log" consists of taking the original system log, copying it, and sending is as en email attachment. Kosugi further discloses that the controller 88 also acquires a system log stored in the non-volatile memory 78 of the baseboard 30, to be specific, a BIOS log in addition to the alarm message indicating the system down during the BOOT processing, and notifies the remote maintenance server 16 of the system log as the attachment file of the electronic mail including the alarm message through the Internet.

In response to appellant's argument (page 6) that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Kosugi teaches substantially all the limitations, except for the idea of "the failure generates a system management interrupt and the BIOS program is triggered in response to the system management interrupt. Davis shows the generation of both

system interrupt and triggering of the timer interrupt in order to detect interrupts during in pre-boot operations.

Regarding Appellant's argument (page 7, first paragraph) that Kosugi and Davis, taken alone or in combination, do not teach or suggest a computer system which includes a system controller coupled between a processor bus and a local bus where the system controller is operable to receive an indication of the critical event and upon receipt of the indication, initiate operation of a timer, and determine whether the BIOS program has written the data to the event log within a configurable period of time defined by the timer much less write the data to the event log if the BIOS program has not written the data to the event log, all as required by claim 17. The Examiner contends that Kosugi and Davis do disclose a system controller coupled between a processor bus and a local bus (see fig. 2A, in which the line that represents the bus from the local CPU connects to the item 88 and another local bus (paragraph [0030], lines 4 - 14). Kosugi also discloses that data is written to the log whether or not BIOS program has not written data to the event log. In order words, data is still written to the log if BIOS program has not written to the event log (Figs. 7A and 7B; see the end of paragraph [0034]).

In response to Appellant's arguments (pages 7, second and third paragraphs) that Kosugi and Davis, taken alone or in combination, do not teach or suggest a method of responding to an event in a computer system having a processor and a system controller where the system controller is coupled between a processor bus and a local bus where the method includes issuing an interrupt to the processor in response to the

event, detecting the interrupt at the system controller coupled to the processor, initiating a timer in the system controller upon detection of the interrupt, and writing data to an event log by executing a BIOS program. The Examiner contends that that Kosugi and Davis do disclose the limitation mentioned above (see Kosugi, figs. 7A and 7B; paragraph 0035 for the description of IMP board, which acts on behalf of the controller 88. In paragraphs [0035] and [0038], the configuration or settings of “timers “is described.

In response to appellants' argument (pages 6 and 7) that the combination of Kosugi and Davis do not teach or suggest the claimed limitations, the examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosure taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170, USPQ 209 (CCPA 1971). references are evaluated by what they suggest to one verse in the art, rather than by their specific disclosures.

In fact, it appears that Appellants are interpreting the claims very narrow without considering the broad teaching of the references used in the rejection.

Appellants are reminded that the examiner is entitled to the broadest reasonable interpretation of the claims. Appellants always have the opportunity to amend the claims during prosecution and broad interpretation by the examiner reduces the

possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater 162 USPQ 541,550-51 (CCPA 1969).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Yves Dalencourt/

Primary Examiner, Art Unit 2457

Conferees:

/Salad Abdullahi/

Primary Examiner, Art Unit 2457

/ARIO ETIENNE/

Supervisory Patent Examiner, Art Unit 2457